Low Distortion Differential RF/IF Amplifier

AD8351

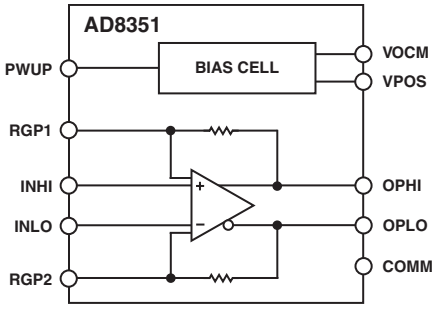
FEATURES

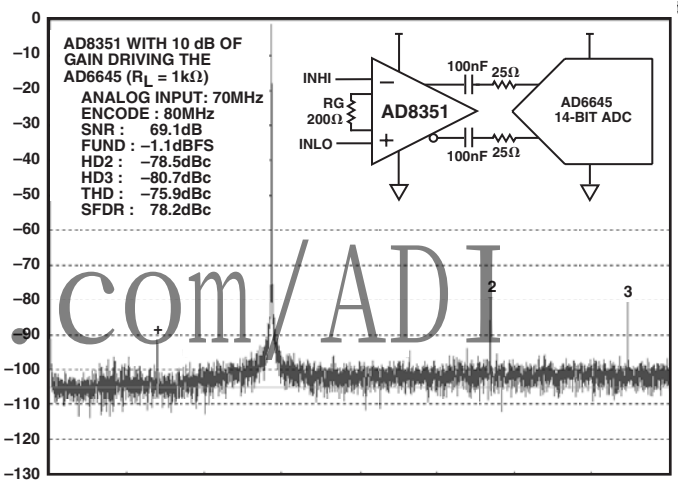
–3 dB Bandwidth of 2.2 GHz for A_V = 12 dB
Single Resistor Programmable Gain
0 dB ≤ A_V ≤ 26 dB
Differential Interface
Low Noise Input Stage 2.7 nV/√Hz @ A_V = 10 dB
Low Harmonic Distortion
–79 dBc Second @ 70 MHz
–81 dBc Third @ 70 MHz
OIP3 of 31 dBm @ 70 MHz
Single-Supply Operation: 3 V to 5.5 V
Low Power Dissipation: 28 mA @ 5 V
Adjustable Output Common-Mode Voltage
Fast Settling and Overdrive Recovery
Slew Rate of 13,000 V/μs
Power-Down Capability
10-Lead MSOP Package

APPLICATIONS

Differential ADC Drivers
Single-Ended-to-Differential Conversion
IF Sampling Receivers
RF/IF Gain Blocks
SAW Filter Interfacing

FUNCTIONAL BLOCK DIAGRAM





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GENERAL DESCRIPTION

The AD8351 is a low cost differential amplifier useful in RF and IF applications up to 2.2 GHz. The voltage gain can be set from unity to 26 dB using a single external gain resistor. The AD8351 provides a nominal 150 Ω differential output impedance. The excellent distortion performance and low noise characteristics of this device allow for a wide range of applications.

The AD8351 is designed to satisfy the demanding performance requirements of communications transceiver applications. The device can be used as a general-purpose gain block, an ADC driver, and a high speed data interface driver, among other functions. The AD8351 can also be used as a single-ended-to-differential amplifier with similar distortion products as in the differential configuration. The exceptionally good distortion performance makes the AD8351 an ideal solution for 12-bit and 14-bit IF sampling receiver designs.

Fabricated in ADI's high speed XFCB process, the AD8351 has high bandwidth that provides high frequency performance and low distortion. The quiescent current of the AD8351 is 28 mA typically. The AD8351 amplifier comes in a compact 10-lead MSOP package and will operate over the temperature range of –40°C to +85°C.

REV. B

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AD8351—SPECIFICATIONS (V_S = 5 V, R_L = 150 Ω, R_G = 110 Ω (A_V = 10 dB), f = 70 MHz, T = 25°C, parameters specified differentially, unless otherwise noted .)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	GAIN = 6 dB, V_{OUT} ≤ 1.0 V p-p		3,000		MHz
	GAIN = 12 dB, V_{OUT} ≤ 1.0 V p-p		2,200		MHz
	GAIN = 18 dB, V_{OUT} ≤ 1.0 V p-p		600		MHz
Bandwidth for 0.1 dB Flatness	0 dB ≤ GAIN ≤ 20 dB, V_{OUT} ≤ 1.0 V p-p		200		MHz
Bandwidth for 0.2 dB Flatness	0 dB ≤ GAIN ≤ 20 dB, V_{OUT} ≤ 1.0 V p-p		400		MHz
Gain Accuracy	Using 1% Resistor for R_G, 0 dB ≤ A_V ≤ 20 dB		±1		dB
Gain Supply Sensitivity	V_S ± 5%		0.08		dB/V
Gain Temperature Sensitivity	–40°C to +85°C		3.9		mdB/°C
Slew Rate	R_L = 1 kΩ, V_{OUT} = 2 V Step		13,000		V/μs
	R_L = 150 Ω, V_S = 2 V Step		7,500		V/μs
Settling Time	1 V Step to 1%		<3		ns
Overdrive Recovery Time	V_{IN} = 4 V to 0 V Step, V_{OUT} ≤ ±10 mV		<2		ns
Reverse Isolation (S12)			–67		dB
INPUT/OUTPUT CHARACTERISTICS					
Input Common-Mode Voltage Adjustment Range			1.2 to 3.8		V
Max Output Voltage Swing	1 dB Compressed		4.75		V p-p
Output Common-Mode Offset			40		mV
Output Common-Mode Drift	–40°C to +85°C		0.24		mV/°C
Output Differential Offset Voltage			20		mV
Output Differential Offset Drift	–40°C to +85°C		0.13		mV/°C
Input Bias Current			±15		μA
Input Resistance[1]			5		kΩ
Input Capacitance[1]			0.8		pF
CMRR			43		dB
Output Resistance[1]			150		Ω
Output Capacitance[1]			0.8		pF
POWER INTERFACE					
Supply Voltage		3		5.5	V
PWUP Threshold			1.3		V
PWUP Input Bias Current	PWUP at 5 V		100		μA
	PWUP at 0 V		25		μA
Quiescent Current			28	32	mA

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Parameter	Conditions	Min	Typ	Max	Unit
NOISE/DISTORTION					
10 MHz					
Second/Third Harmonic Distortion[2]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		–95/–93		dBc
	R_L = 150 Ω, V_{OUT} = 2 V p-p		–86/–71		dBc
Third-Order IMD	R_L = 1 kΩ, f1 = 9.5 MHz, f2 = 10.5 MHz, V_{OUT} = 2 V p-p Composite		–90		dBc
	R_L = 150 Ω, f1 = 9.5 MHz, f2 = 10.5 MHz, V_{OUT} = 2 V p-p Composite		–70		dBc
Output Third-Order Intercept	f1 = 9.5 MHz, f2 = 10.5 MHz		33		dBm
Noise Spectral Density (RTI)			2.65		nV/√Hz
1 dB Compression Point			13.5		dBm
70 MHz					
Second/Third Harmonic Distortion[2]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		–79/–81		dBc
	R_L = 150 Ω, V_{OUT} = 2 V p-p		–65/–66		dBc
Third-Order IMD	R_L = 1 kΩ, f1 = 69.5 MHz, f2 = 70.5 MHz, V_{OUT} = 2 V p-p Composite		–85		dBc
	R_L = 150 Ω, f1 = 69.5 MHz, f2 = 70.5 MHz, V_{OUT} = 2 V p-p Composite		–69		dBc
Output Third-Order Intercept	f1 = 69.5 MHz, f2 = 70.5 MHz		31		dBm
Noise Spectral Density (RTI)			2.70		nV/√Hz
1 dB Compression Point			13.3		dBm
140 MHz					
Second/Third Harmonic Distortion[2]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		–69/–69		dBc
	R_L = 150 Ω, V_{OUT} = 2 V p-p		–54/–53		dBc
Third-Order IMD	R_L = 1 kΩ, f1 = 139.5 MHz, f2 = 140.5 MHz, V_{OUT} = 2 V p-p Composite		–79		dBc
	R_L = 150 Ω, f1 = 139.5 MHz, f2 = 140.5 MHz, V_{OUT} = 2 V p-p Composite		–67		dBc
Output Third-Order Intercept	f1 = 139.5 MHz, f2 = 140.5 MHz		29		dBm
Noise Spectral Density (RTI)			2.75		nV/√Hz
1 dB Compression Point			13		dBm
240 MHz					
Second/Third Harmonic Distortion[2]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		–60/–66		dBc
	R_L = 150 Ω, V_{OUT} = 2 V p-p		–46/–50		dBc
Third-Order IMD	R_L = 1 kΩ, f1 = 239.5 MHz, f2 = 240.5 MHz, V_{OUT} = 2 V p-p Composite		–76		dBc
	R_L = 150 Ω, f1 = 239.5 MHz, f2 = 240.5 MHz, V_{OUT} = 2 V p-p Composite		–62		dBc
Output Third-Order Intercept	f1 = 239.5 MHz, f2 = 240.5 MHz		27		dBm
Noise Spectral Density (RTI)			2.90		nV/√Hz
1 dB Compression Point			13		dBm

NOTES
[1]Values are specified differentially.
[2]See Applications section for single-ended-to-differential performance.

Specifications subject to change without notice.

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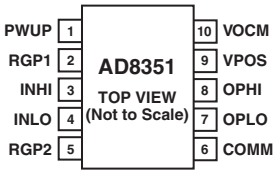
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPOS . . . . . 6 V
PWUP Voltage . . . . . VPOS
Internal Power Dissipation . . . . . 320 mW
θ_{JA} . . . . . 125°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temp. Range	Package Description	Package Option	Branding
AD8351ARM	–40°C to +85°C	10-Lead MSOP, 7" Tape and Reel	RM-10	JDA
AD8351ARM-R2	–40°C to +85°C	10-Lead MSOP, 7" Tape and Reel	RM-10	JDA
AD8351ARM-REEL7	–40°C to +85°C	10-Lead MSOP, 7" Tape and Reel	RM-10	JDA
AD8351-EVAL		Evaluation Board		

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	PWUP	Apply a positive voltage (1.3 V ≤ V_{PWUP} ≤ VPOS) to activate device.
2	RGP1	Gain Resistor Input 1.
3	INHI	Balanced Differential Input. Biased to midsupply, typically ac-coupled
4	INLO	Balanced Differential Input. Biased to midsupply, typically ac-coupled.
5	RGP2	Gain Resistor Input 2.
6	COMM	Device Common. Connect to low impedance ground.
7	OPLO	Balanced Differential Output. Biased to VOCM, typically ac-coupled.
8	OPHI	Balanced Differential Output. Biased to VOCM, typically ac-coupled.
9	VPOS	Positive Supply Voltage. 3 V to 5.5 V.
10	VOCM	Voltage applied to this pin sets the common-mode voltage at both the input and output. Typically decoupled to ground with a 0.1 μF capacitor.

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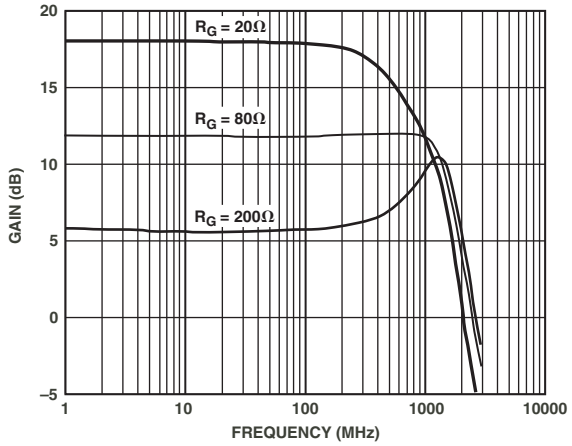
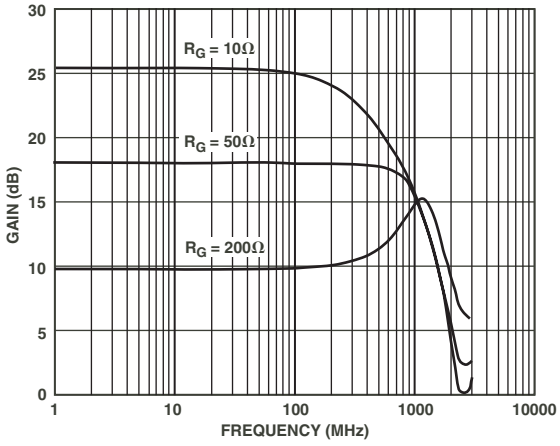
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8351 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

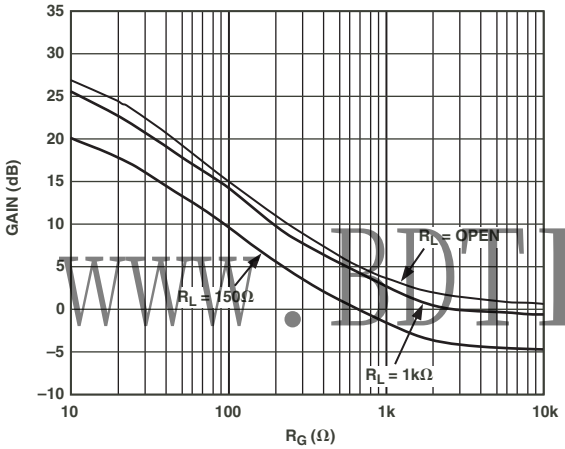
(V_S = 5 V, T = 25°C, unless otherwise noted.)



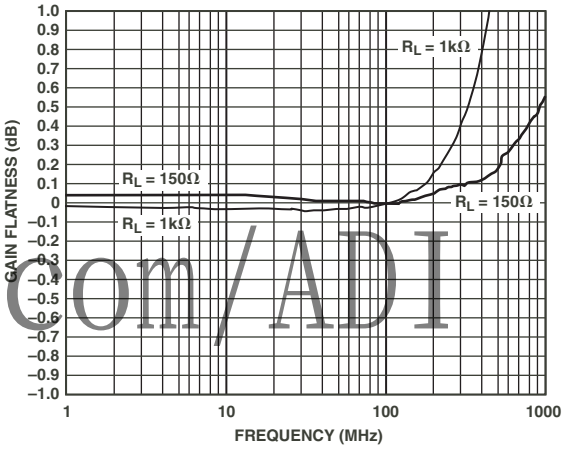
TPC 1. Gain vs. Frequency for a 150 Ω Differential Load (A_V = 6 dB, 12 dB, and 18 dB)



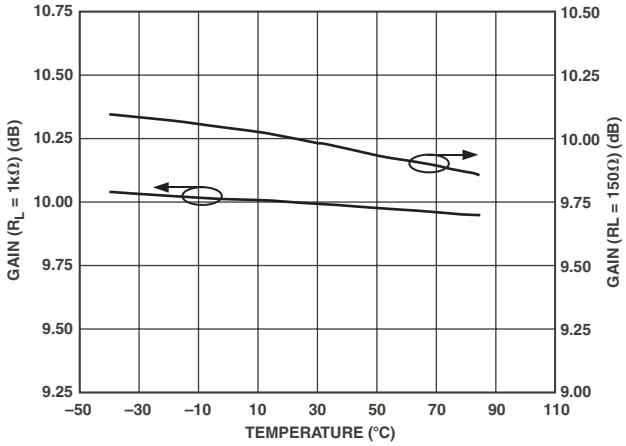
TPC 4. Gain vs. Frequency for a 1 kΩ Differential Load (A_V = 10 dB, 18 dB, and 26 dB)



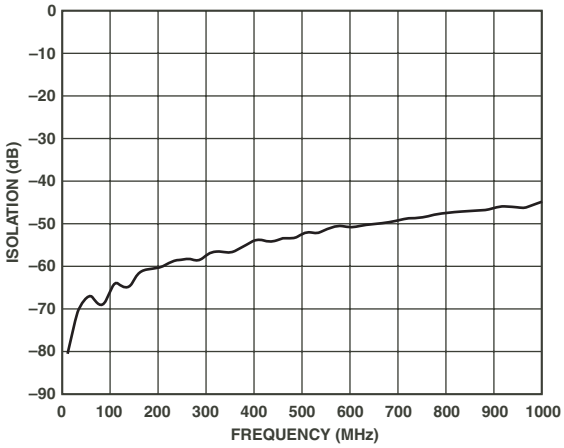
TPC 2. Gain vs. Gain Resistor, R_G (f = 100 MHz, R_L = 150 Ω, 1 kΩ, and Open)



TPC 5. Gain Flatness vs. Frequency (R_L = 150 Ω and 1 kΩ, A_V=10 dB)



TPC 3. Gain vs. Temperature at 100 MHz (A_V = 10 dB)



TPC 6. Isolation vs. Frequency (A_V = 10 dB)

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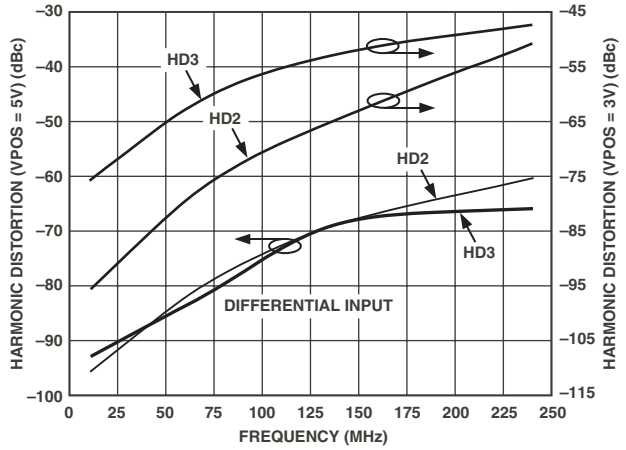
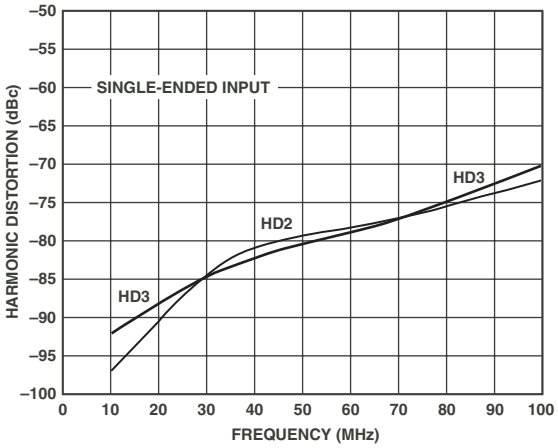
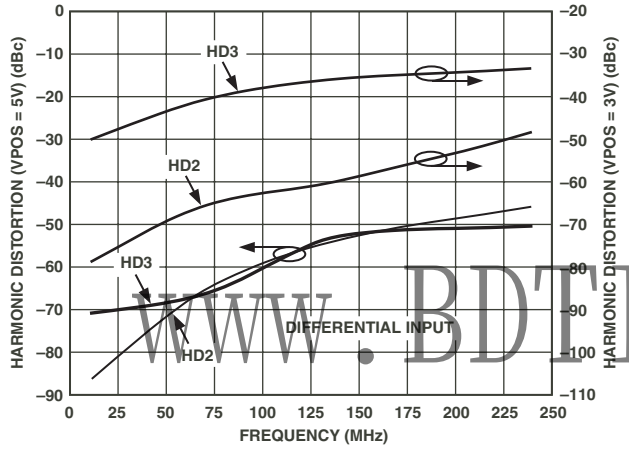


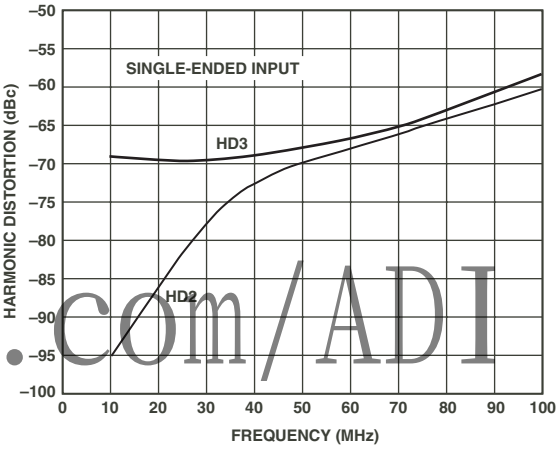
TPC 7. Harmonic Distortion vs. Frequency for 2 V p-p into R_L = 1 kΩ (A_V = 10 dB, at 3 V and 5 V Supplies)



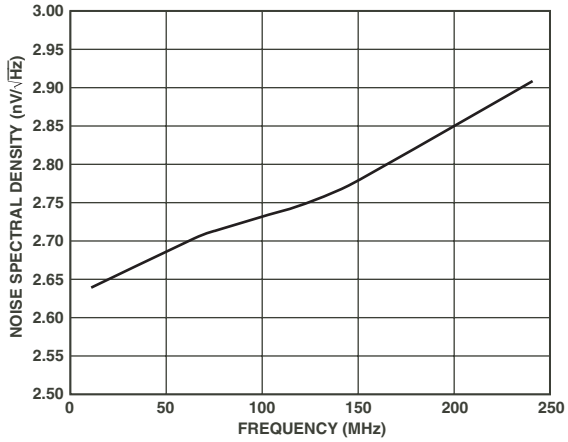
TPC 10. Harmonic Distortion vs. Frequency for 2 V p-p into R_L = 1 kΩ Using Single-Ended Input (A_V = 10 dB)



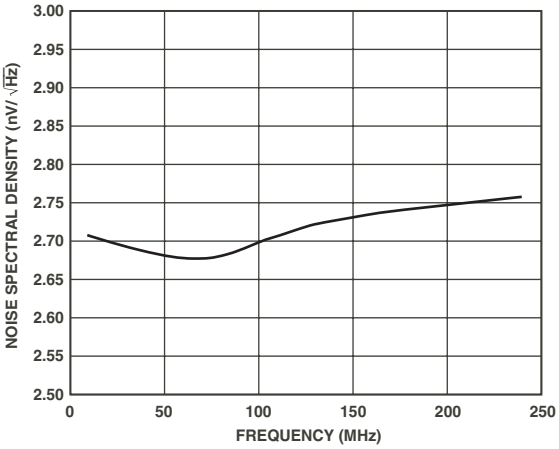
TPC 8. Harmonic Distortion vs. Frequency for 2 V p-p into R_L = 150 Ω (A_V = 10 dB, at 3 V and 5 V Supplies)



TPC 11. Harmonic Distortion vs. Frequency for 2 V p-p into R_L = 150 Ω Using Single-Ended Input (A_V = 10 dB)



TPC 9. Noise Spectral Density (RTI) vs. Frequency (R_L = 150 Ω, 5 V Supply, A_V = 10 dB)



TPC 12. Noise Spectral Density (RTI) vs. Frequency (R_L = 150 Ω, 3 V Supply, A_V = 10 dB)

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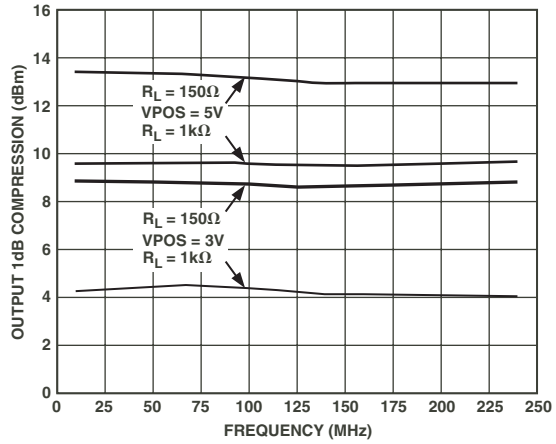
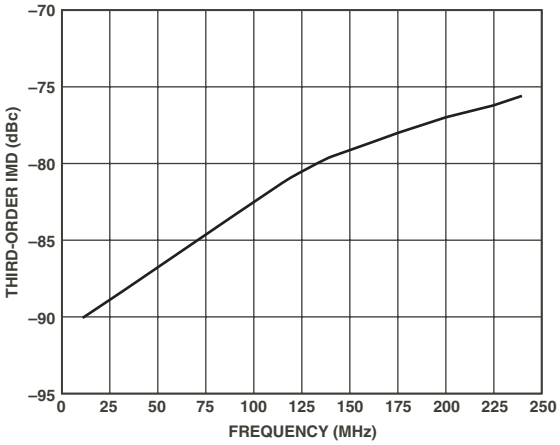
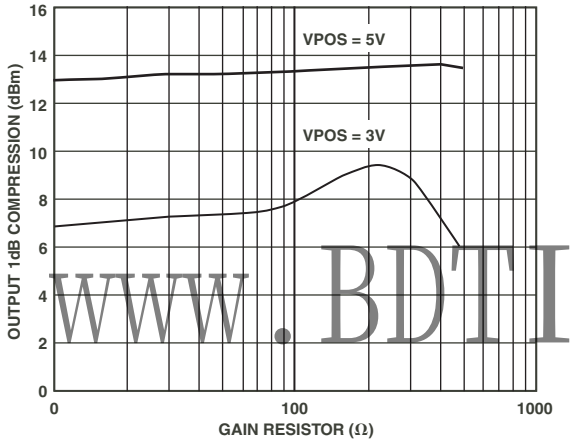


TPC 13. Output Compression Point, P1 dB, vs. Frequency (R_L = 150 Ω and 1 kΩ, A_V = 10 dB, at 3 V and 5 V Supplies)



TPC 16. Third-Order Intermodulation Distortion vs. Frequency for a 2 V p-p Composite Signal into R_L = 1 kΩ (A_V = 10 dB, at 5 V Supplies)



TPC 14. Output Compression Point, P1 dB, vs. R_G (f = 100 MHz, R_L = 150 Ω, A_V = 10 dB, at 3 V and 5 V Supplies)

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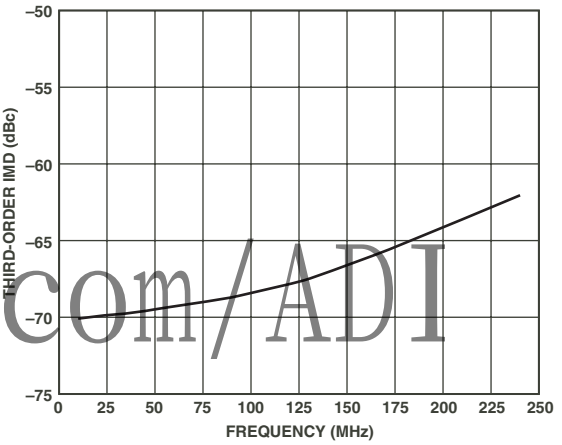
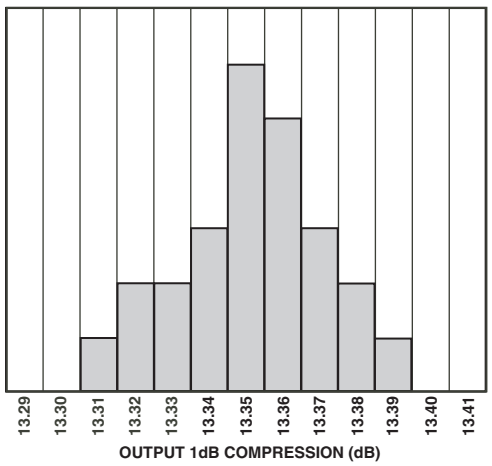
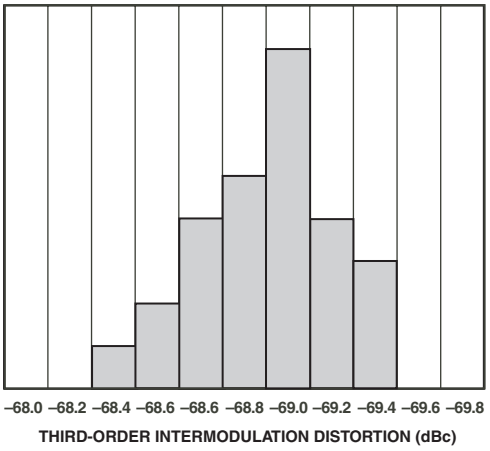


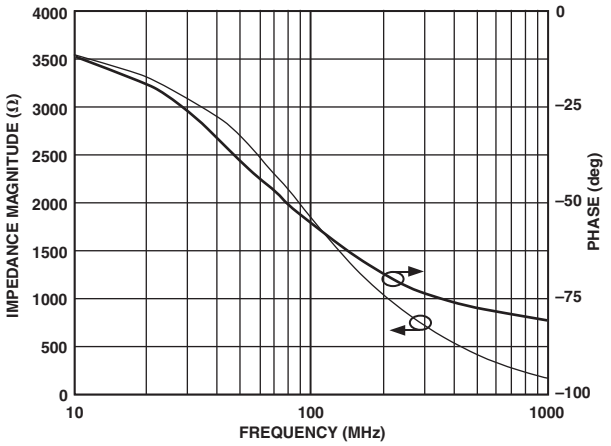
TPC 17. Third-Order Intermodulation Distortion vs. Frequency for a 2 V p-p Composite Signal into R_L = 150 Ω (A_V = 10 dB, at 5 V Supplies)



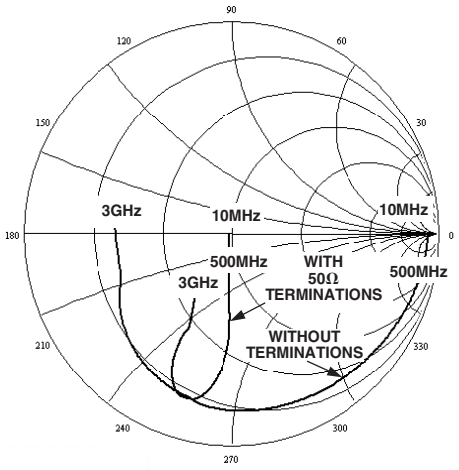
TPC 15. Output Compression Point Distribution (f = 70 MHz, R_L = 150 Ω, A_V = 10 dB)



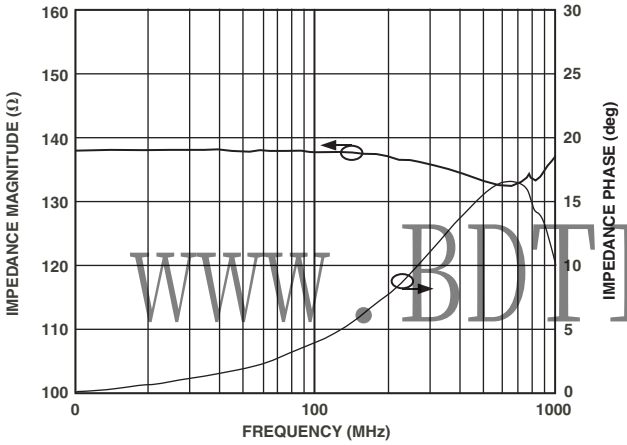
TPC 18. Third-Order Intermodulation Distortion Distribution (f = 70 MHz, R_L = 150 Ω, A_V = 10 dB)



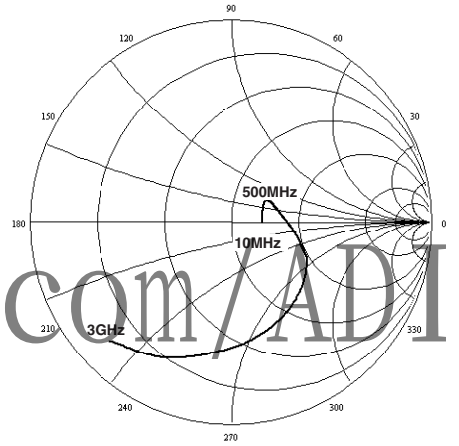
TPC 19. Input Impedance vs. Frequency



TPC 22. Input Reflection Coefficient vs. Frequency ($R_S = R_L = 100\ \Omega$ with and without 50 Ω Terminations)



TPC 20. Output Impedance vs. Frequency



TPC 23. Output Reflection Coefficient vs. Frequency ($R_S = R_L = 100\ \Omega$)

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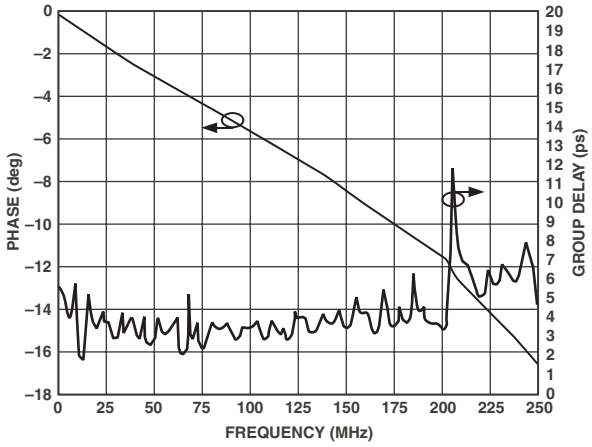
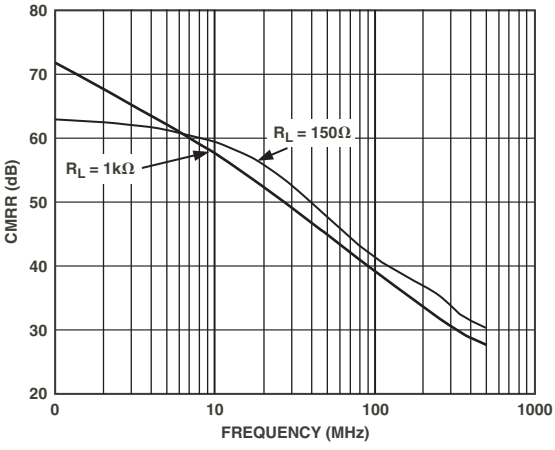
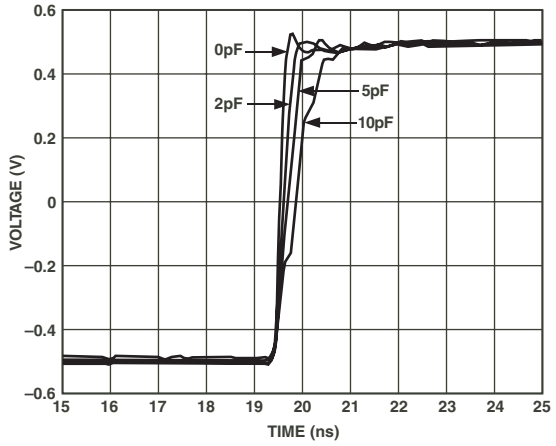


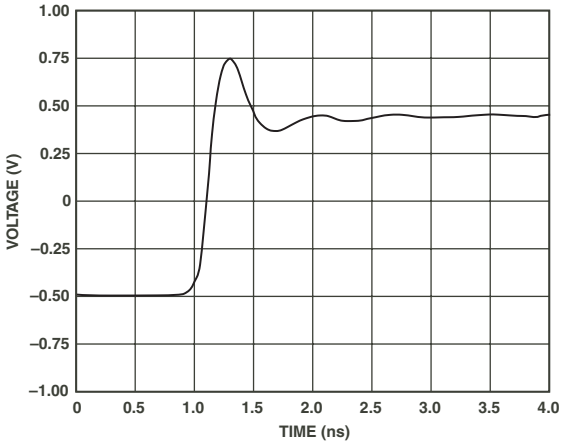
TPC 21. Phase and Group Delay (A_V = 10 dB, at 5 V Supplies)



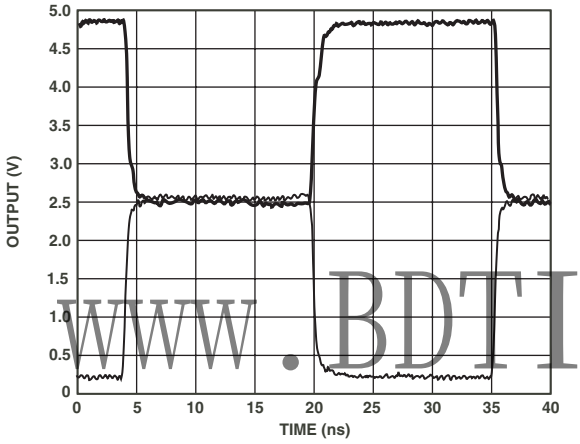
TPC 24. Common-Mode Rejection Ratio, CMRR ($R_S = 100\ \Omega$)



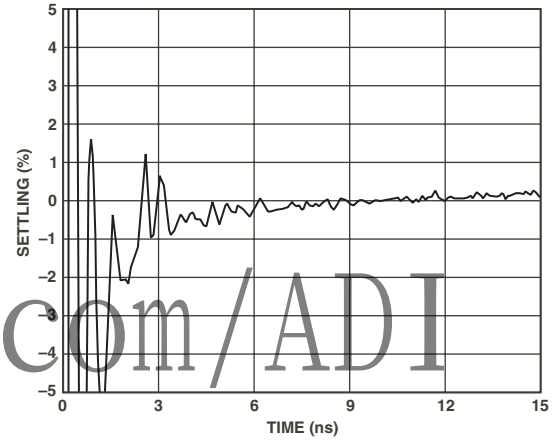
TPC 25. Transient Response under Capacitive Loading (R_L = 150 Ω, C_L = 0 pF, 2 pF, 5 pF, 10 pF)



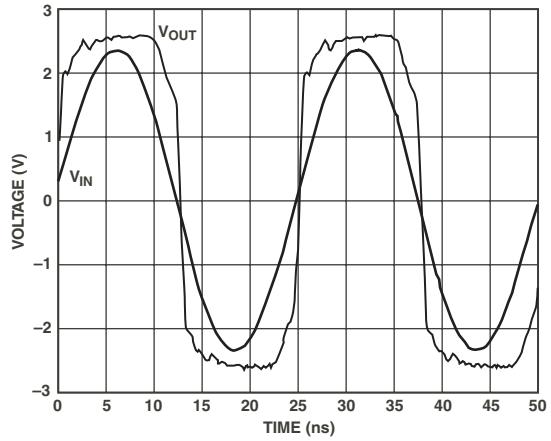
TPC 28. Large Signal Transient Response for a 1 V p-p Output Step (A_V = 10 dB, R_{IP} = 25 Ω)



TPC 26. 2× Output Overdrive Recovery (R_L = 150 Ω, A_V = 10 dB)



TPC 29. 1% Settling Time for a 2 V p-p Step (A_V = 10 dB, R_L = 150 Ω)



TPC 27. Overdrive Recovery Using Sinusoidal Input Waveform R_L = 150 Ω (A_V = 10 dB, at 5 V Supplies)

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BASIC CONCEPTS

Differential signaling is used in high performance signal chains, where distortion performance, signal-to-noise ratio, and low power consumption is critical. Differential circuits inherently provide improved common-mode rejection and harmonic distortion performance as well as better immunity to interference and ground noise.

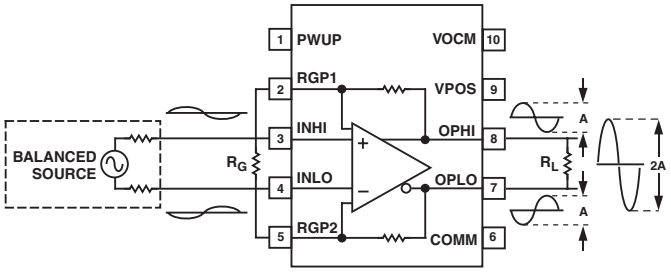

Figure 1. Differential Circuit Representation

Figure 1 illustrates the expected input and output waveforms for a typical application. Usually the applied input waveform will be a balanced differential drive, where the signal applied to the INHI and INLO pins are equal in amplitude and differ in phase by 180°. In some applications, baluns may be used to transform a single-ended drive signal to a differential signal. The AD8351 may also be used to transform a single-ended signal to a differential signal.

GAIN ADJUSTMENT

The differential gain of the AD8351 is set using a single external resistor, R_G, which is connected between Pins 2 and 5. The gain can be set to any value between 0 dB and 26 dB using the resistor values specified in TPC 2, with common gain values provided in Table I. The board traces used to connect the external gain resistor should be balanced and as short as possible to help prevent noise pickup and to ensure balanced gain and stability. The low frequency voltage gain of the AD8351 can be modeled as

$$A_V = \frac{R_L \times R_G(5.6) + 9.2 \times R_F \times R_L}{R_G \times R_L \times 4.6 + 19.5 \times R_G + (R_L + R_F) \times (39 + R_G)} = \left| \frac{V_{OUT}}{V_{IN}} \right|$$

where: R_F is 350 Ω (internal).

R_L is the single-ended load resistance.

R_G is the gain setting resistor.

Table I. Gain Resistor Selection for Common Gain Values (Load Resistance Is Specified as Single-Ended)

Gain, A_V	R_G (R_L = 75 Ω)	R_G (R_L = 500 Ω)
0 dB	680 Ω	2 kΩ
6 dB	200 Ω	470 Ω
10 dB	100 Ω	200 Ω
20 dB	22 Ω	43 Ω

COMMON-MODE ADJUSTMENT

The output common-mode voltage level is the dc offset voltage present at each of the differential outputs. The ac signals are of equal amplitude with a 180° phase difference but are centered at the same common-mode voltage level. The common-mode output voltage level can be adjusted from 1.2 V to 3.8 V by driving the desired voltage level into the VOCM pin, as illustrated in Figure 2.

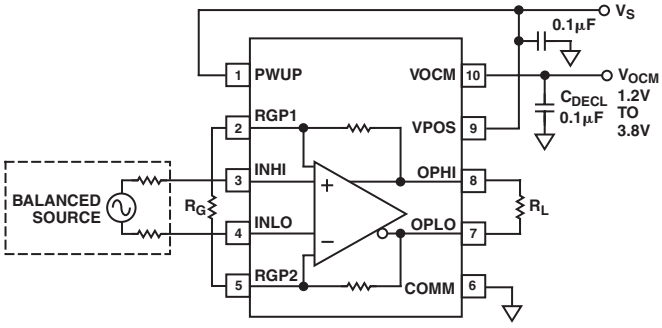

Figure 2. Common-Mode Adjustment

INPUT AND OUTPUT MATCHING

The AD8351 provides a moderately high differential input impedance of 5 kΩ. In practical applications, the input of the AD8351 will be terminated to a lower impedance to provide an impedance match to the driving source, as depicted in Figure 3. The terminating resistor, R_T, should be as close as possible to the input pins in order to minimize reflections due to impedance mismatch. The 150 Ω output impedance may need to be transformed to provide the desired output match to a given load. Matching components can be calculated using a Smith Chart or by using a resonant approach to determine the matching network that results in a complex conjugate match. The input and output impedances and reflection coefficients are provided in TPCs 19, 20, 22, and 23. For additional information on reactive matching to differential sources and loads, refer to the Applications section of the AD8350 data sheet.

Figure 3 illustrates a SAW (surface acoustic wave) filter interface. Many SAW filters are inherently differential, allowing for a low loss output match. In this example, the SAW filter requires a 50 Ω source impedance in order to provide the desired center frequency and Q. The series L shunt C output network provides a 150 Ω to 50 Ω impedance transformation at the desired frequency of operation. The impedance transformation is illustrated on a Smith Chart in Figure 4.

It is possible to drive a single-ended SAW filter simply by connecting the unused output to ground using the appropriate terminating resistance. The overall gain of the system will be reduced by 6 dB due to the fact that only half of the signal will be available to the input of the SAW filter.

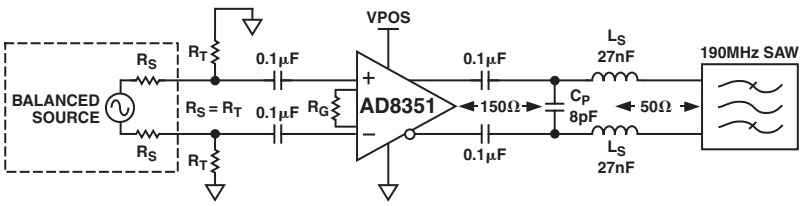

Figure 3. Example of Differential SAW Filter Interface (f_C = 190 MHz)

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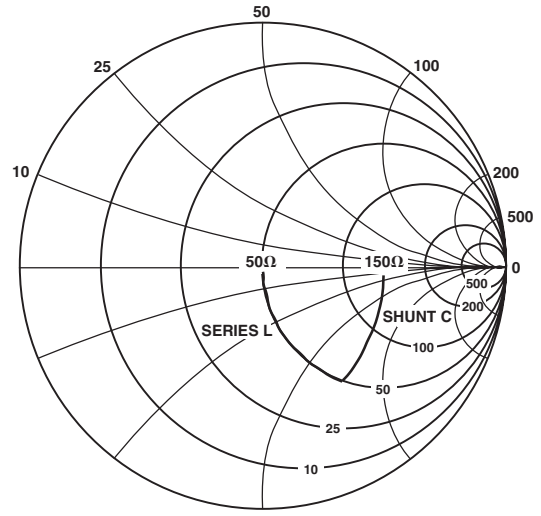

Figure 4. Smith Chart Representation of SAW Filter Output Matching Network

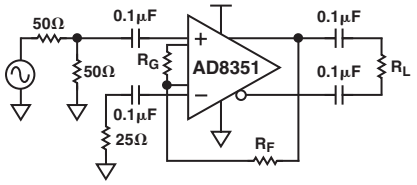

Figure 5. Single-Ended Application

SINGLE-ENDED-TO-DIFFERENTIAL OPERATION

The AD8351 can easily be configured as a single-ended-to-differential gain block, as illustrated in Figure 5. The input signal is ac-coupled and applied to the INHI input. The unused input is ac-coupled to ground. The values of C1 through C4 should be selected such that their reactances are negligible at the desired frequency of operation. To balance the outputs, an external feedback resistor, R_F, is required. To select the gain resistor and the feedback resistor, refer to Figures 6a and 6b. From Figure 6a, select an R_G for the required dB gain at a given load. Next, select from Figure 6b an R_F resistor for the selected R_G and load.

Even though the differential balance is not perfect under these conditions, the distortion performance is still impressive. TPCs 10 and 11 show the second and third harmonic distortion performance when driving the input of the AD8351 using a single-ended 50 Ω source.

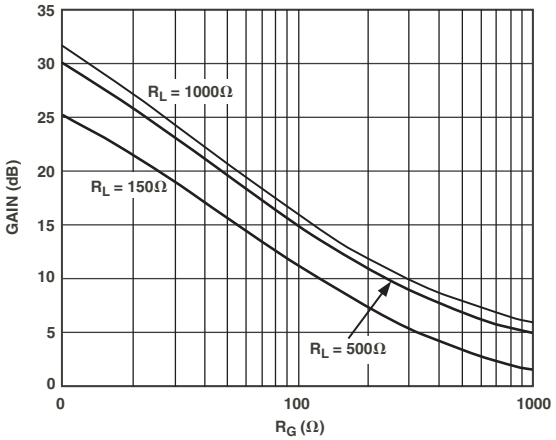

Figure 6a. Gain Selection

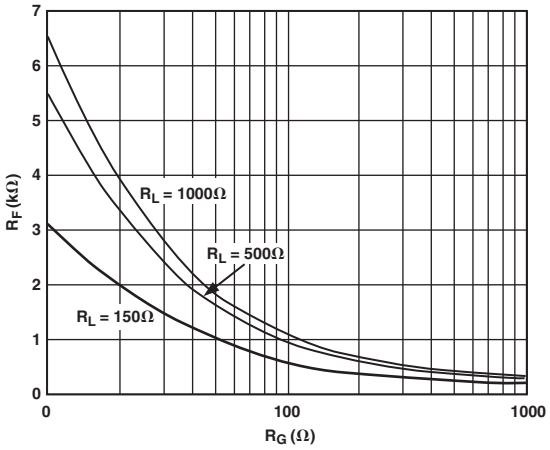

Figure 6b. Feedback Resistor Selection

ADC DRIVING

The circuit in Figure 7 represents a simplified front end of the AD8351 driving the AD6645, which is a 14-bit, 105 MSPS A/D converter. For optimum performance, the AD6645 and the AD8351 are driven differentially. The resistors R1 and R2 present a 50 Ω differential input impedance to the source with R3 and R4 providing isolation from the A/D input. The gain setting resistor for the AD8351 is R_G. The AD6645 presents a 1 kΩ differential load to the AD8351 and requires a 2.2 V p-p differential signal between AIN and $\overline{\text{AIN}}$ for a full-scale output. This AD8351 circuit then provides the gain, isolation, and source matching for the AD6645. The AD8351 also provides a balanced input, not provided by the balun, to the AD6645, which is essential for second-order cancellation. The signal generator is bipolar, centered around ground. Connecting the VOCM pin (10) of the AD8351 to the VREF pin of the AD6645 sets the common-mode output voltage of the AD8351 at 2.4 V. This voltage is bypassed with a 0.1 μF capacitor. Increasing the gain of the AD8351 will increase the system noise and thus decrease the SNR but will not significantly affect the distortion. The circuit in Figure 7 can provide SFDR performance of better than –90 dBc with a 10 MHz input and –80 dBc with a 70 MHz input at a gain of 10 dB.

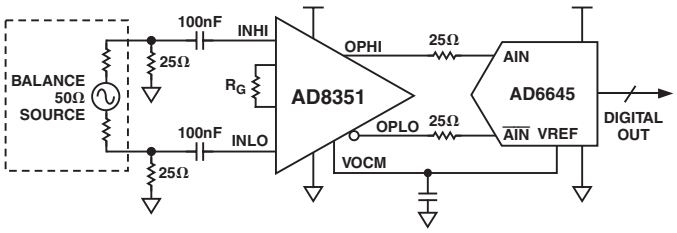

Figure 7. ADC Driving Application Using Differential Input

The circuit of Figure 8 represents a single-ended input to differential output configuration of the AD8351 driving the AD6645. In this case, R1 provides the input impedance. R_G is the gain setting resistor. The resistor R_F is required to balance the output voltages required for second-order cancellation by the AD6645 and can be selected using a chart. (See the Single-Ended-to-Differential Operation section.) The circuit depicted in Figure 8 can provide SFDR performance of better than –90 dBc with a 10 MHz input and –77 dBc with a 70 MHz input.

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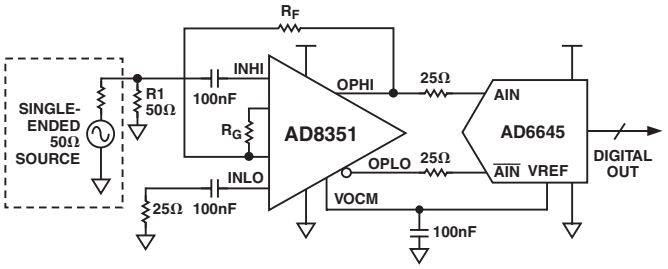

Figure 8. ADC Driving Application Using Single-Ended Input

ANALOG MULTIPLEXING

The AD8351 can be used as an analog multiplexer in applications where it is desirable to select multiple high speed signals. The isolation of each device when in a disabled state (PWUP pin pulled low) is about 60 dBc for the maximum input level of 0.5 V p-p out to 100 MHz. The low output noise spectral density allows for a simple implementation as depicted in Figure 9. The PWUP interface can be easily driven using most standard logic interfaces. By using an N-bit digital interface, up to N devices can be controlled. Output loading effects and noise need to be considered when using a large number of input signal paths. Each disabled AD8351 presents approximately a 700 Ω load in parallel with the 150 Ω output source impedance of the enabled device. As the load increases due to the addition of N devices, the distortion performance will degrade due to the heavier loading. Distortion better than –70 dBc can be achieved with four devices muxed into a 1 kΩ load for signal frequencies up to 70 MHz.

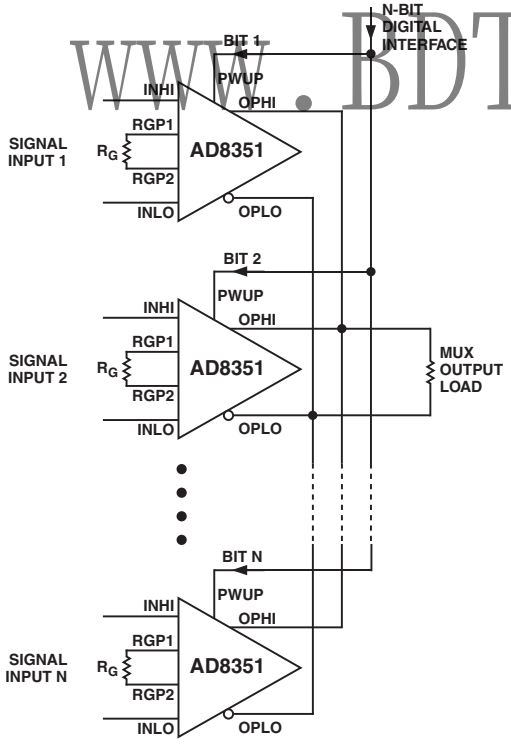

Figure 9. Using Several AD8351s to Form an N-Channel Analog MUX

I/O CAPACITIVE LOADING

Input or output direct capacitive loading greater than a few picofarads can result in excessive peaking and/or oscillation outside the pass band. This results from the package and bond wire inductance resonating in parallel with the input/output capacitance of the device and the associated coupling that results internally through the ground inductance. For low resistive load or source resistance, the effective Q is lower, and higher relative capacitance termination(s) can be allowed before oscillation or excessive peaking occurs. These effects can be eliminated by adding series input resistors (R_{IP}) for high source capacitance, or series output resistors (R_{OP}) for high load capacitance. Generally less than 25 Ω is all that is required for I/O capacitive loading greater than ~2 pF. The higher the C, the smaller the R parasitic suppression resistor required. In addition, R_{IP} also helps to reduce low gain in-band peaking, especially for light resistive loads.

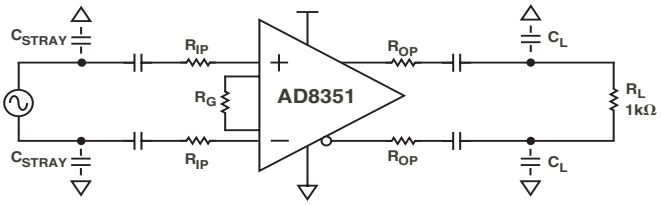

Figure 10. Input and Output Parasitic Suppression Resistors, R_{IP} and R_{OP}, Used to Suppress Capacitive Loading Effects

Due to package parasitic capacitance on the R_G ports, high R_G values (low gain) cause high ac-peaking inside the pass band, resulting in poor settling in the time domain. As an example, when driving a 1 kΩ load, using 25 Ω for R_{IP} reduces the peaking by ~7 dB for R_G equal to 200 Ω (A_V = 10 dB) (see Figure 11).

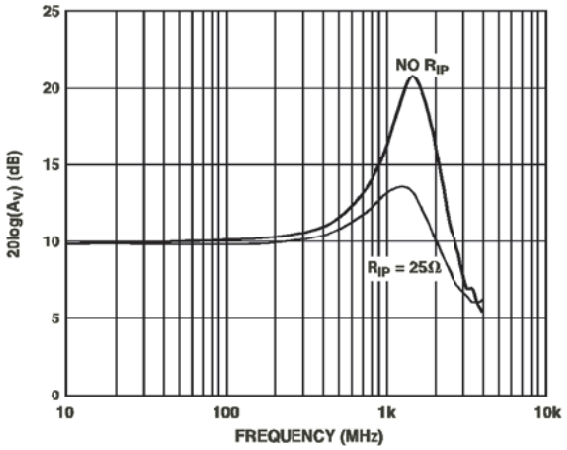

Figure 11. Reducing Gain Peaking with Parasitic Suppressing Resistors (R_{IP} = 25 Ω, R_L = 1 kΩ)

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It is important to ensure that all I/O, ground, and R_G port traces be kept as short as possible. In addition, it is required that the ground plane be removed from under the package. Due to the inverse relationship between the gain of the device and the value of the R_G resistor, any parasitic capacitance on the R_G ports can result in gain-peaking at high frequencies. Following the precautions outlined in Figure 12 will help to reduce parasitic board capacitance, thus extending the device's bandwidth and reducing potential peaking or oscillation.

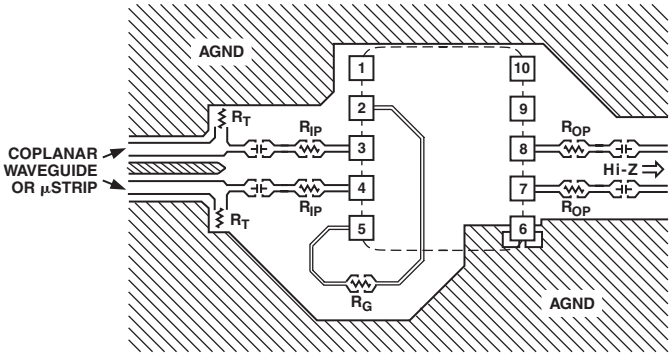

Figure 12. General Description of Recommended Board Layout for High-Z Load Conditions

TRANSMISSION LINE EFFECTS

As noted, stray transmission line capacitance, in combination with package parasitics, can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking. R_F transmission lines connecting the input and output networks should be designed such that stray capacitance is minimized. The output single-ended source impedance of the AD8351 is dynamically set to a nominal value of 75 Ω. Therefore, for a matched load termination, the characteristic impedance of the output transmission lines should be designed to be 75 Ω. In many situations, the final load impedance may be relatively high, greater than 1 kΩ. It is suggested that the board be designed as shown in Figure 12 for high impedance load conditions. In most practical board designs, this requires that the printed-circuit board traces be dimensioned to a small width (~5 mils) and that the underlying and adjacent ground planes are far enough away to minimize capacitance.

Typically the driving source impedance into the device will be low and terminating resistors will be used to prevent input reflections. The transmission line should be designed to have the appropriate characteristic impedance in the low-Z region. The high impedance environment between the terminating resistors and device input pins should not have ground planes underneath or near the signal traces. Small parasitic suppressing resistors may be necessary at the device input pins to help desensitize ("de-Q") the resonant effects of the device bond wires and surrounding parasitic board capacitance. Typically, 25 Ω series resistors (size 0402) adequately de-Q the input system without a significant decrease in ac performance.

Figure 13 illustrates the value of adding input and output series resistors to help desensitize the resonant effects of board parasitics. Overshoot and undershoot can be significantly reduced with the simple addition of R_{IP} and R_{OP}.

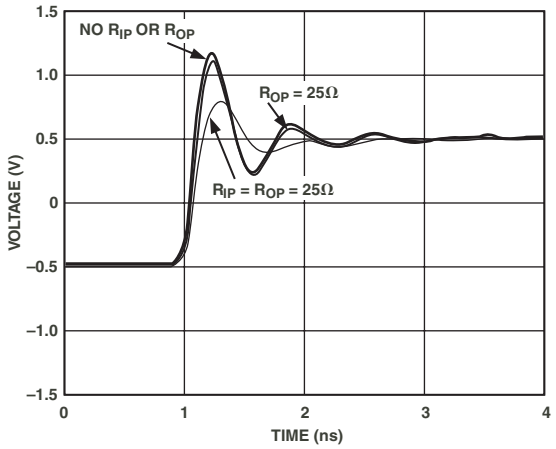

Figure 13. Step Response Characteristics with and without Input and Output Parasitic Suppression Resistors

CHARACTERIZATION SETUP

The test circuit used for 150 Ω and 1 kΩ load testing is provided in Figure 14. The evaluation board uses balun transformers to simplify interfacing to single-ended test equipment. Balun effects need to be removed from the measurements in order to accurately characterize the performance of the device at frequencies exceeding 1 GHz.

The output L-pad matching networks provide a broadband impedance match with minimum insertion loss. The input lines are terminated with 50 Ω resistors for input impedance matching. The power loss associated with these networks needs to be accounted for when attempting to measure the gain of the device. The required resistor values and the appropriate insertion loss and correction factors used to assess the voltage gain are provided in Table II.

Table II. Load Conditions Specified Differentially

Load Condition	R1	R2	Total Insertion Loss	Conversion Factor 20 log (S21) to 20 log (A_V)
150 Ω	43.2 Ω	86.6 Ω	5.8 dB	7.6 dB
1 kΩ	475 Ω	52.3 Ω	15.9 dB	25.9 dB

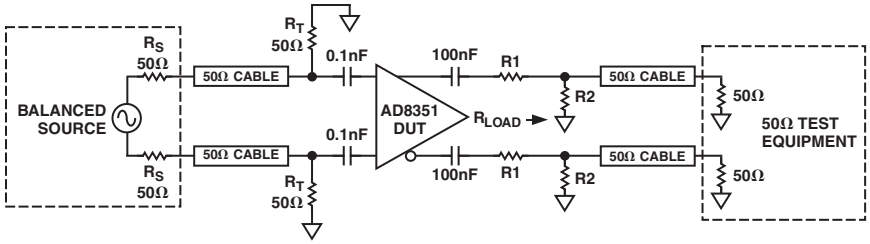

Figure 14. Test Circuit

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EVALUATION BOARD

An evaluation board is available for experimentation. Various parameters such as gain, common-mode level, and input and output network configurations can be modified through minor resistor changes. The schematic and evaluation board artwork are presented in Figures 15, 16, and 17.

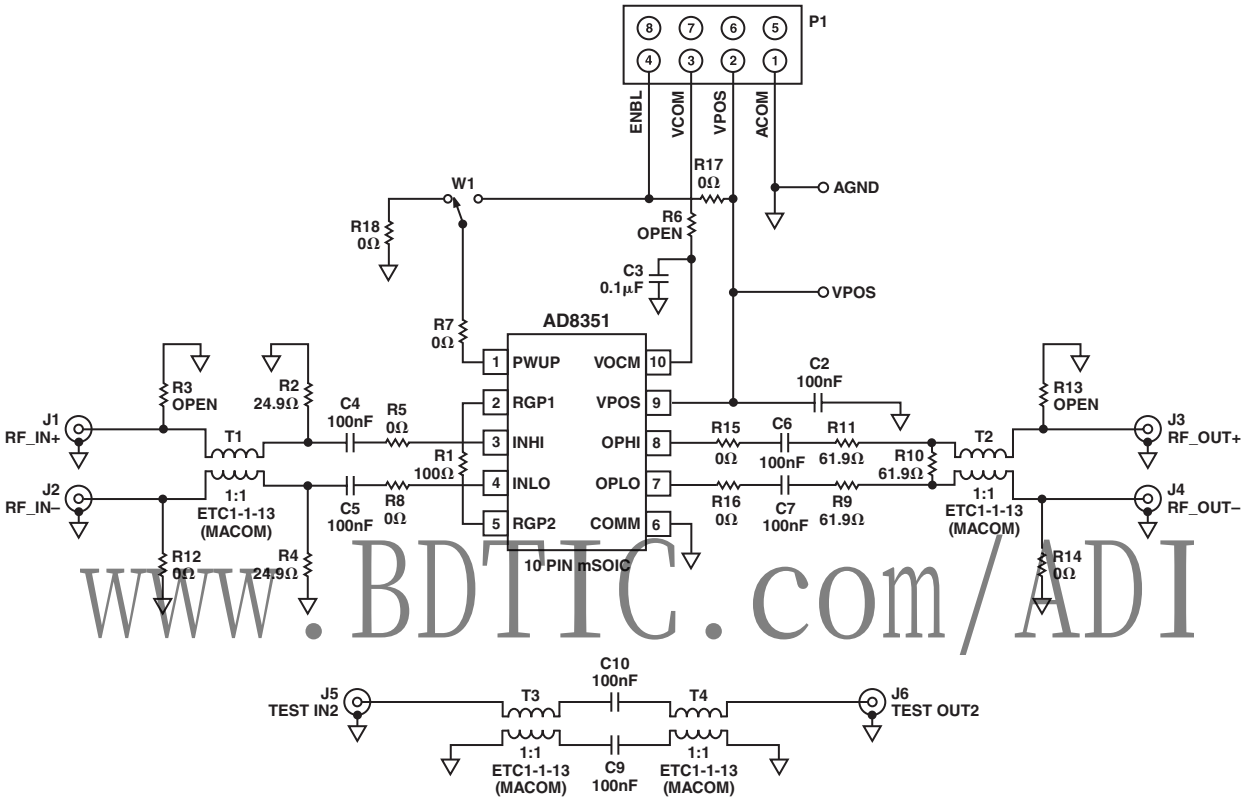

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Figure 15. Evaluation Board Schematic

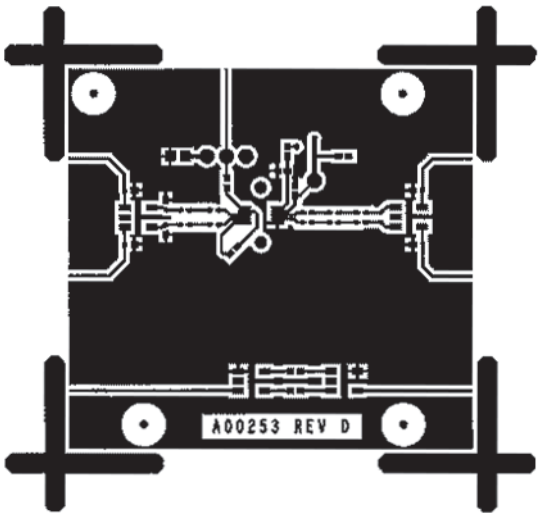

Figure 16. Component Side Layout

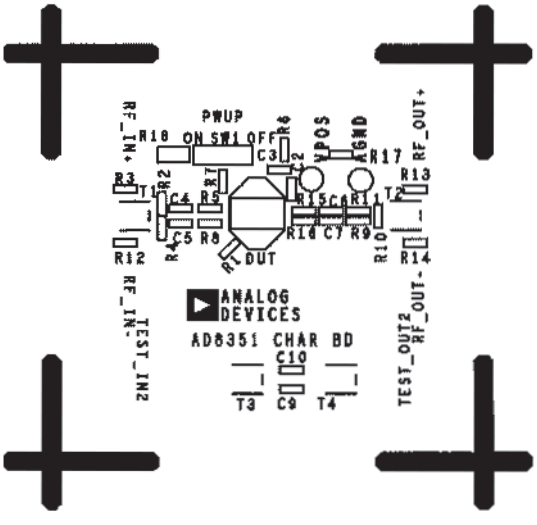

Figure 17. Component Side Silkscreen

Table III. Evaluation Board Configuration Options

Component	Function	Default Condition
P1-1, P1-2, VPOS, AGND	Supply and Ground Pins.	Not Applicable
P1-3	Common-Mode Offset Pin. Allows for monitoring or adjustment of the output common-mode voltage.	Not Applicable
W1, R7, P1-4, R17, R18	Device Enable. Configured such that switch W1 disables the device when Pin 1 is set to ground. Device can be disabled remotely using Pin 4 of header P1.	W1 = Installed R7 = 0 Ω (Size 0603) R17 = R18 = 0 Ω (Size 0603)
R2, R3, R4, R5, R8, R12, T1, C4, C5	Input Interface. R3 and R12 are used to ground one side of the differential drive interface for single-ended applications. T1 is a 1-to-1 impedance ratio balun used to transform a single-ended input into a balanced differential signal. R2 and R4 are used to provide a differential 50 Ω input termination. R5 and R8 can be increased to reduce gain peaking when driving from a high source impedance. The 50 Ω termination provides an insertion loss of 6 dB. C4 and C5 are used to provide ac coupling.	R2 = R4 = 24.9 Ω (Size 0805) R3 = Open (Size 0603) R5 = R8 = R12 = 0 Ω (Size 0603) C4 = C5 = 10 0 nF (Size 0603) T1 = Macom™ ETC1-1-13
R9, R10, R11, R13, R14, R15, R16, T2, C4, C5, C6, C7	Output Interface. R13 and R14 are used to ground one side of the differential output interface for single-ended applications. T2 is a 1-to-1 impedance ratio balun used to transform a balanced differential signal into a single-ended signal. R9, R10, and R11 are provided for generic placement of matching components. R15 and R16 allow additional output series resistance when driving capacitive loads. The evaluation board is configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of 9.9 dB. C4 through C7 are used to provide ac coupling.	R9 = R10 = 61.9 Ω (Size 0603) R11 = 61.9 Ω (Size 0603) R13 = Open (Size 0603) R14 = 0 Ω (Size 0603) R15 = R16 = 0 Ω (Size 0402) C4 = C5 = 100 nF (Size 0603) C6 = C7 = 100 nF (Size 0603) T2 = Macom ETC1-1-13
R1	Gain Setting Resistor. Resistor R1 is used to set the gain of the device. Refer to TPC 2 when selecting gain resistor. When R1 is 100 Ω, the overall system gain of the evaluation board will be approximately –6 dB.	R1 = 100 Ω (Size 0603)
C2	Power Supply Decoupling. The supply decoupling consists of a 100 nF capacitor to ground.	C2 = 100 nF (Size 0805)
R6, C3, P1-3	Common-Mode Offset Adjustment. Used to trim common-mode output level. By applying a voltage to Pin 3 of header P1, the output common-mode voltage can be directly adjusted. Typically decoupled to ground using a 0.1 μF capacitor.	R6 = 0 Ω (Size 0603) C3 = 0.1 μF (Size 0805)
T3, T4, C9, C10	Calibration Networks. Calibration path provided to allow for compensation of the insertion loss of the baluns and the reactance of the coupling capacitors.	T3 = T4 = Macom ETC1-1-13 C9 = C10 = 100 nF (Size 0603)

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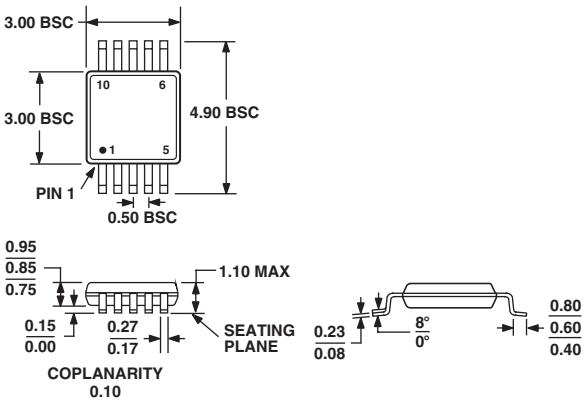
OUTLINE DIMENSIONS

10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187BA

C03145–0–2/04(B)

Revision History

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Location	Page
2/04—Data Sheet changed from REV. A to REV. B.	
Changes to ORDERING GUIDE	4
Changes to TPC 4	5
3/03—Data Sheet changed from REV. 0 to REV. A.	
Change to ORDERING GUIDE	4
Change to Table III	15